Dual N-Channel 75-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
75	0.048 @ V_{GS} = 10 V	4.8
	0.062 @ V_{GS} = 4.5 V	4.2

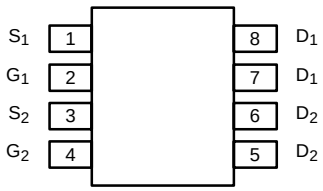
FEATURES

- TrenchFET® Power MOSFET
- 175°C Maximum Junction Temperature
- High-Efficiency PWM Optimized

APPLICATIONS

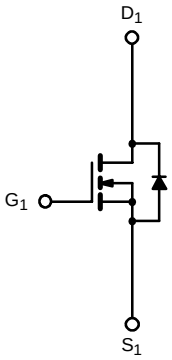
- Automotive Such As:
  - High-Side Switch
  - Motor Drives
  - 42-V Battery

SO-8

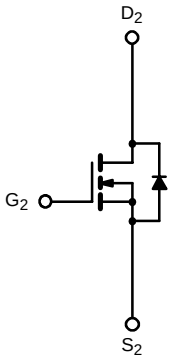


Top View

Ordering Information: Si4992EY—E3
Si4992EY-T1—E3 (with Tape and Reel)



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	75		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current (T_J = 175°C)[a]	T_A = 25°C	I_D	4.8	3.6	A
	T_A = 85°C		3.7	2.8	
Continuous Source Current[a]		I_S	2	1.1	
Pulsed Drain Current		I_{DM}	20		
Avalanche Current	L = 0.1 mH	I_{AS}	8		
Single Avalanche Energy (Duty Cycle ≤ 1%)		E_{AS}	3.2		mJ
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.4	1.4	W
	T_A = 85°C		1.4	0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175		°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	50	62.5	°C/W
	Steady State		85	110	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	31	37	

Notes
a. Surface Mounted on 1” x 1” FR4 Board.

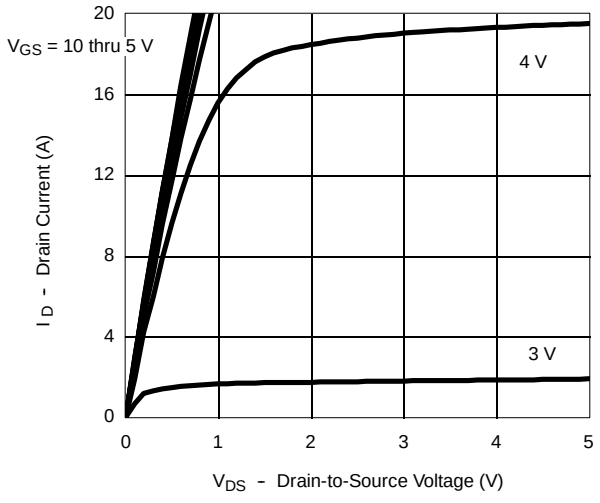
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1		3	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 75 V, V_{GS} = 0 V			1	μA
		V_{DS} = 75 V, V_{GS} = 0 V, T_J = 85°C			20	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 4.8 A		0.039	0.048	Ω
		V_{GS} = 4.5 V, I_D = 4.2 A		0.050	0.062	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 4.8 A		16		S
Diode Forward Voltage[a]	V_{SD}	I_S = 2.4 A, V_{GS} = 0 V		0.8	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 38 V, V_{GS} = 10 V, I_D = 4.8 A		14	21	nC
Gate-Source Charge	Q_{gs}			2.4		
Gate-Drain Charge	Q_{gd}			3.5		
Gate Resistance	R_g	f = 1 MHz		3.6		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 38 V, R_L = 38 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_g = 6 Ω		7	15	ns
Rise Time	t_r			10	15	
Turn-Off Delay Time	$t_{d(off)}$			22	35	
Fall Time	t_f			10	15	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2.4 A, di/dt = 100 A/μs		25	50	

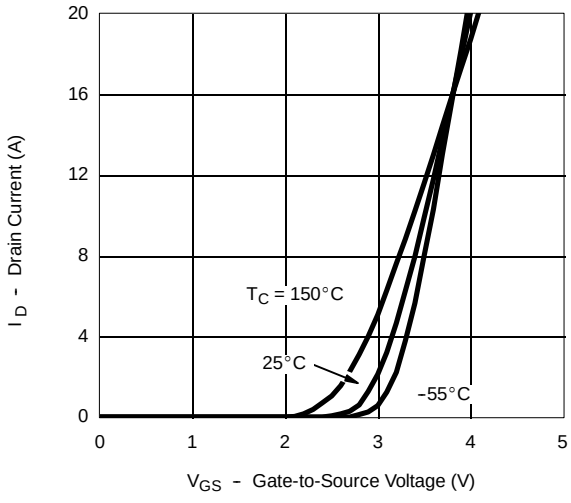
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics

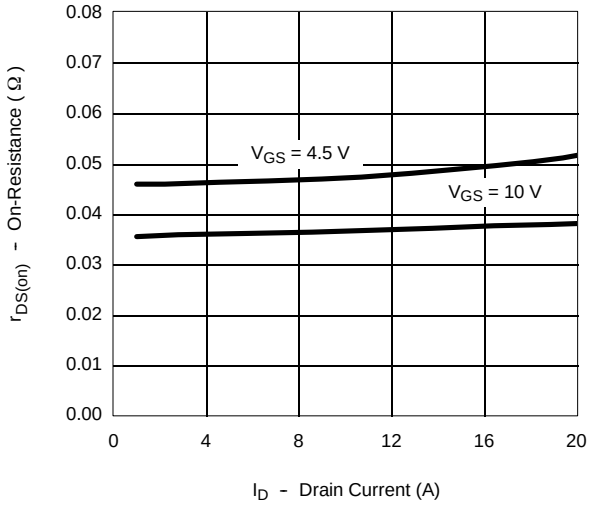


Transfer Characteristics

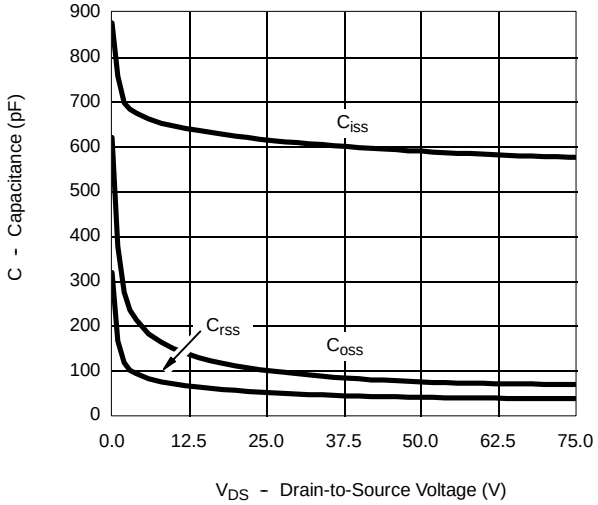


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

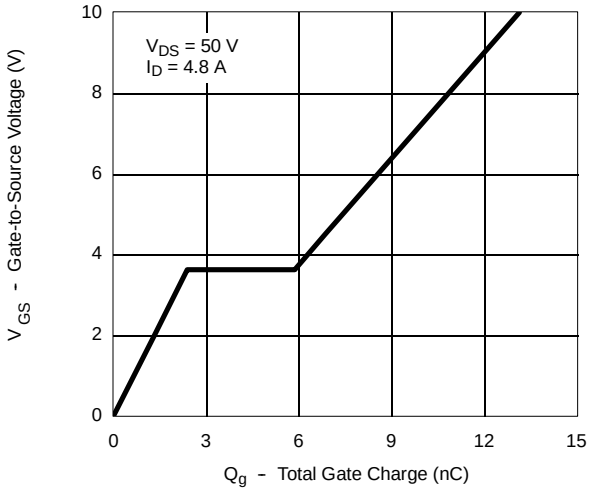
On-Resistance vs. Drain Current



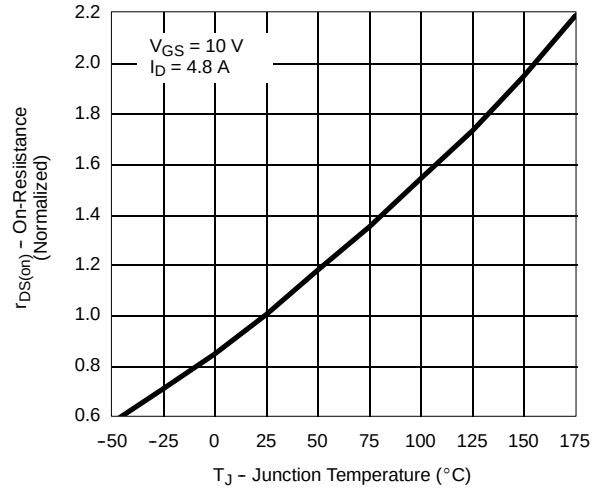
Capacitance



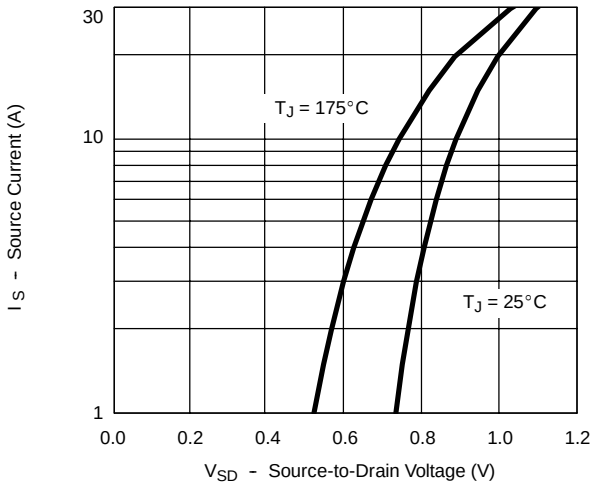
Gate Charge



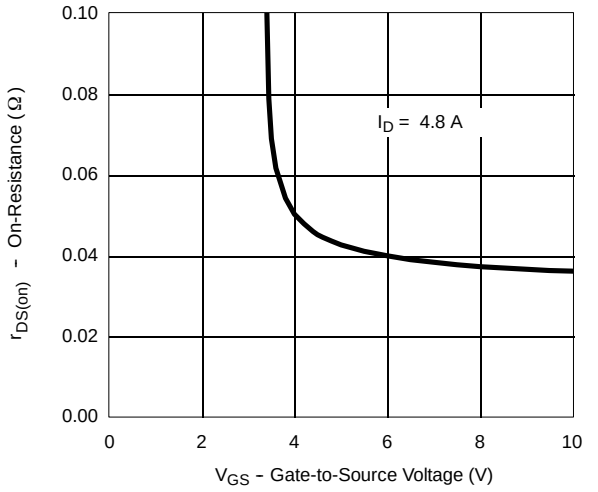
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

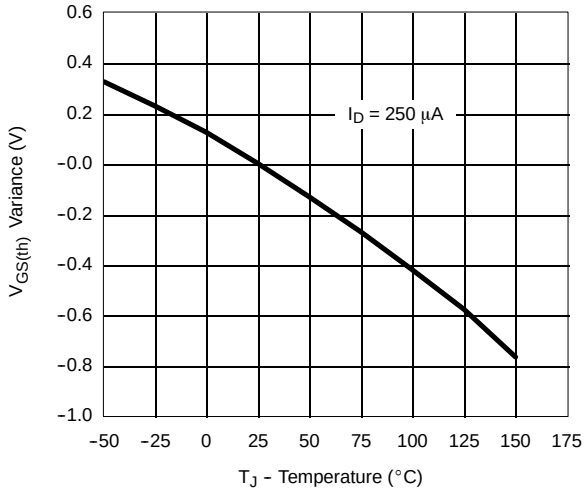


On-Resistance vs. Gate-to-Source Voltage

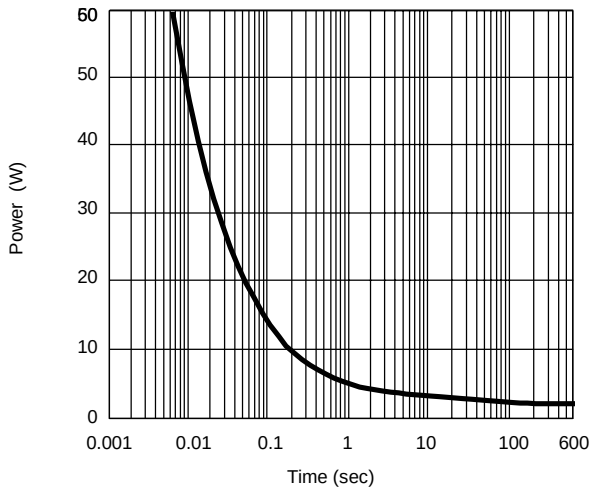


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

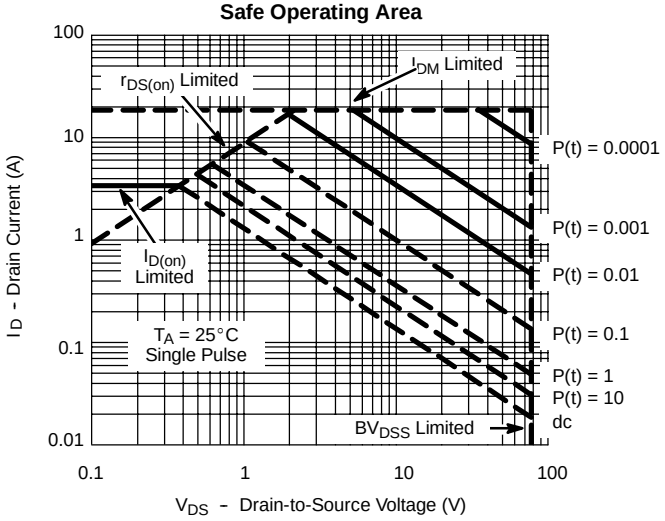
Threshold Voltage



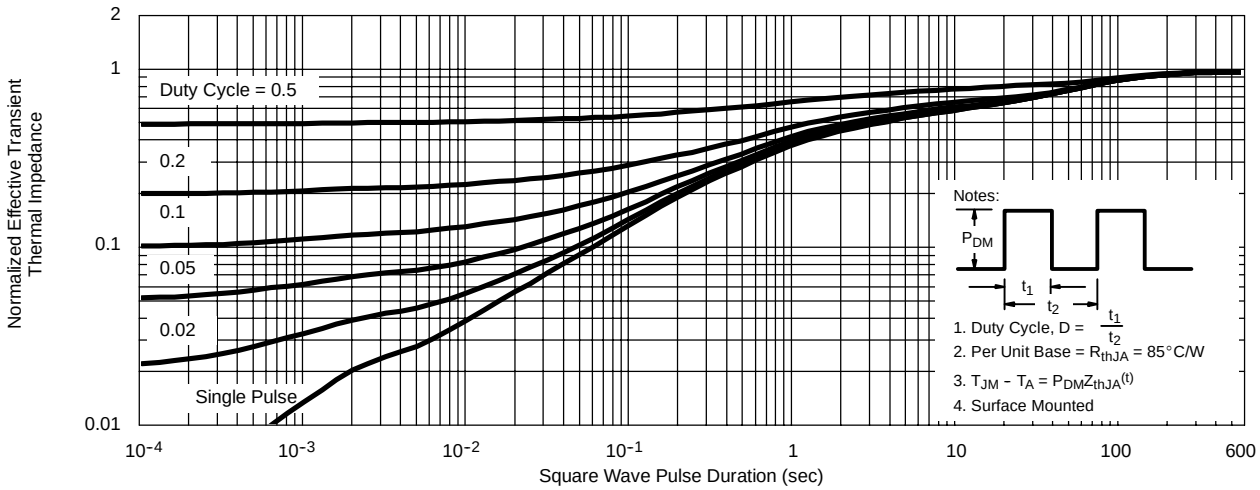
Single Pulse Power



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)